A 250 W Audio Amplifier with Straightforward Digital Input– PWM Output Conversion

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Abstract

A switching audio amplifier which features high output power (250 W), high efficiency (90 %) while performing a 96 dB dynamic range is presented. The amplifier is based on a single-chip integrated circuit that converts a digital input data stream at frequency f_s into an $8f_s$ Pulse Width Modulated (PWM) output power signal, without using intermediate filter. An embedded I^2S input interface is capable of receiving digital words up to 24-bit at a rate f_s ranging from 32 kHz to 48 kHz. The chip is fabricated with a 0.6 µm Bipolar-CMOS-DMOS (BCD) technology and assembled in a surface-mount package. Due to the high output power, it drives four external power MOS transistors.

1. Introduction

In the last few years the use of digital technology in audio electronics has become widespread and, nowadays, there is an increasing interest in the development of completely digital audio systems. Moreover, the growing market demand for small size multimedia systems with high output power and large number of audio channels, is driving the need for high efficiency power amplifiers. Recently, a great effort has been made to develop fully digital power amplifiers, usually referred to as power DACs. These amplifiers convert the PCM (Pulse Coded Modulation) digital signal into a sigma-delta (Σ–Δ) modulated 1-bit data stream [1] or a PWM (Pulse Width Modulation) signal [2]. The high frequency two-level signal is then amplified using an open loop power buffer and low-pass filtered. This approach is relatively simple, but the output analog signal is adversely affected by supply noise and non-idealities within the power buffer. A good performance can be obtained using more complex digital structures and algorithms for noise and distortion reduction. However, a more efficient approach for building a low cost power DAC relies on the use of a feedback power buffer.

A single-chip power DAC with a feedback power buffer has been recently proposed by K. Philips et al. [3]. The digital input signal is converted in a noise-shaped one-bit signal (Pulse Density Modulation, PDM) using a Σ–Δ modulator. The PDM bitstream directly feeds a class-D amplifier, and a simple LC filter reconstructs the audio signal. The main disadvantage of this approach is the high frequency ($64f_s$) of the PDM signal that causes a rather poor system efficiency. In addition, the high and variable switching frequency makes PDM-based converters quite sensitive to clock jitter and asymmetry between pulse rise and fall time [4].

In order to overcome these disadvantages, we propose a new power DAC that exploits a low-frequency ($8f_s$) PWM signal in the conversion process. This modulation technique, compared to the previous solution, leads to reduced switching losses and lower noise due to the clock jitter. Fabricated with a 0.6 µm BCD technology, the power DAC has an output power of 250 W on 4 Ω, with a 96 dB dynamic range and a 90 % efficiency.

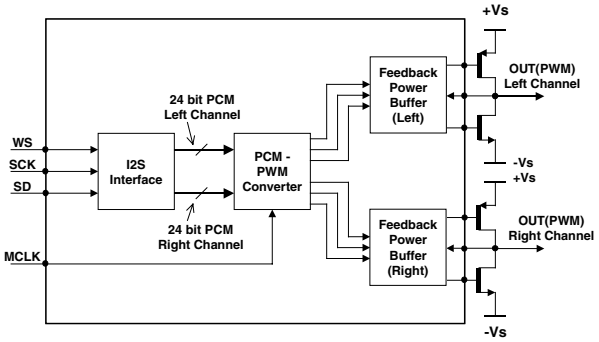

Figure 1. Simplified block diagram of the amplifier

2. Amplifier structure

The amplifier block diagram is shown in Fig. 1. The I^2S interface converts the serial format in a 24-bit sample word at a frequency f_s. The PCM 24-bit words are converted into low-frequency PWM signals by the PCM-PWM block, which is clocked by an external $256f_s$ master clock (MCLK). A "Feedback Power Buffer" then generates a high-power PWM signal. Due to the high output power level, four discrete MOS transistors have been used. Fig. 2 shows the detailed schematic of the PCM-PWM converter. The interpolator increases the PCM input signal frequency from f_s to $16f_s$. The signal is then fed to the noise shaper, which

reduces the in band quantization noise and splits each PCM word in two shorter words of 6-bit each, namely LSB and MSB. The PWM modulators generate three output signals for each channel: PWM_{MSB}, PWM_{LSBp} and PWM_{LSBn}.

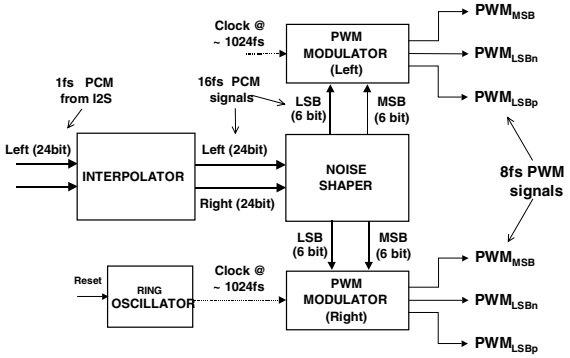

Figure 2. PCM-PWM Converter

These signals are generated using a pulse width double-side, two-level uniform sampling modulation [5]. The main waveforms in the PWM modulator are shown in Fig. 3.

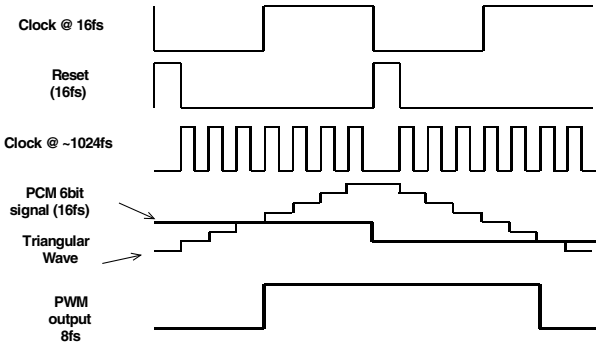

Figure 3. PWM modulator waveforms

The PWM signal frequency is $8f_s$ since consecutive samples modulate each edge of the pulse. Besides limiting the PWM frequency, this modulation technique eliminates even-order harmonics [6]. At the same time, the noise shaper works at $16f_s$ thus providing a good dynamic range.

The PWM signals are fed to the Feedback Power Buffer, which provides a PWM wave at $8f_s$ (F_{PWM}) to the LC filter. When the system operates in stereo mode each Feedback Power Buffer processes one channel, while in bridge configuration they generate two signals with opposite polarity.

3. Noise-Shaper and PWM modulator

Direct PWM conversion of a 24-bit word would imply an unfeasibly high clock rates in the modulator counter; noise shaping is therefore exploited to reduce the number of bits applied to the PWM unit. Different aspects have to be considered in the noise shaper design:

1. maximum allowable clock rate for the selected technology, that is, in our case, 50 MHz for a 6-bit counter. This figure would allow a maximum f_s of 48 kHz with a 6-bit PWM modulator;
2. in-band signal to noise ratio, which has to be at least 96 dB. This requirement must cope with a relatively low Over Sampling Ratio (OSR), which is mandatory for achieving a high system efficiency (i.e., low F_{PWM},);
3. quantization noise out of the audio band, which has to be as low as possible in order not to degrade the system performance.

Fig. 4 shows the noise shaper internal structure. This block acts as a 3rd-order 9-bit noise shaper, thus introducing low out-of-band noise and no idle tones, and it performs a good attenuation of the audio band quantization noise. The noise introduced from the 6-bit quantizer is cancelled by summing the MSB and LSB words, according to the expression:

$$MSB(z) + LSB(z) = PCM_{IN}(z) + Q_{9bit}(z)(1 - z^{-1})^3 + \underline{\underline{+ Q_{6bit}(z)(1 - z^{-1}) - Q_{6bit}(z)(1 - z^{-1})}}$$

The Feedback Power Buffer block, schematically shown in Fig. 5, performs this sum.

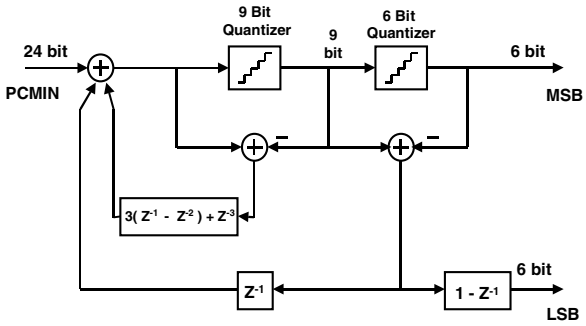

Figure 4. Noise shaper block diagram

As shown in Fig. 5, the inputs of each Feedback Power Buffer are three PWM signals; the first is generated by the modulation of MSB and the other two are generated by the modulation of LSB and –LSB.
MSB is a 6-bit word, which represents the re-quantized input word, while LSB carries the information related to the shaped quantization noise. Even when the input signal is well below the saturation level, LSB has a value near half dynamic and it is a pseudo-random noise. In this condition, the PWM modulation of MSB exhibits a "clean" spectrum, while the PWM modulation of LSB is critical. A remarkable improvement in the conversion of LSB is achieved by phase shifting modulation, which reduces the intermodulation product [5]. To this end, PWM_{LSBn} is inverted and summed to PWM_{LSBp} at the buffer input, thus achieving a three level PWM signal with double frequency.

In order to perform the noise cancellation, the ratio between the amplitude of PWM_{MSB} and PWM_{LSBp} (or

PWM_{LSBn}) must be 1/16 (see Fig. 5); this is achieved by scaling the input resistors appropriately. This ratio would be inaccurate in practice, due to the unavoidable resistor mismatch. We therefore introduced a further 1st-order shaping on the 6-bit quantization noise in order to attenuate the mismatch effect. This solution insures Dynamic Range of 106 dB even with a resistor mismatch around 2%, which can be easy achieved without a complex resistor layout.

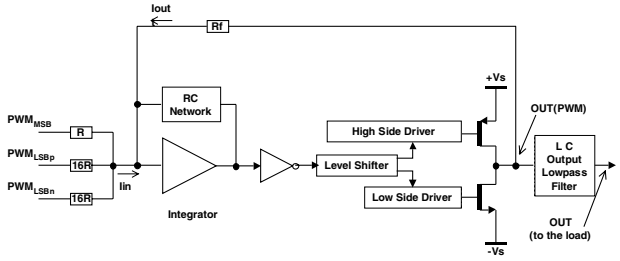

Figure 5. Feedback Power Buffer Block Diagram

4. Feedback Power Buffer

The Feedback Power Buffer, whose internal structure is shown in Fig. 5, behaves as a switching amplifier whose frequency is forced by the two-level PWM signal (PWM_{MSB}) coming from the PCM-PWM converter. Besides carrying information, PWM_{MSB} defines the output switching frequency. Due to the integrator, the feedback forces the average value of currents Iin and Iout to be equal; as a consequence, any errors introduced in the power stage due to power supply fluctuations, dead-times, non ideal edges, MOS non idealities, etc. are rejected.

Thanks to the Feedback Power Buffer gain, the saturation of the output PWM power signal (i.e., 100 % duty cycle) is obtained with a PWM_{MSB} wave modulated at 70 % duty-cycle. It is indeed of the utmost importance to avoid the saturation of the input PWM signals for three main reasons:

1. since the PCM-PWM converter works in open loop, it introduces a PWM typical noise in the audio band, which becomes considerable as saturation is approached;
2. practical implementations of the PWM modulator require a 44 MHz (16 x f_s x 2^6) clock. Since the maximum duty cycle is 70 %, the 30 % residual time interval can be used to reset a free running ring oscillator. In this case no PLL is needed to obtain the high frequency clock, as shown in Fig. 3, and asynchronous conversion is carried out without spurious signals thanks to the resetting;
3. a nearly saturated PWM_{MSB} signal would not be correctly reproduced, due to the finite propagation time in the feedback power buffer.

In order to improve the efficiency, reliability and minimize the noise on the board the external MOS cross-conduction has to be avoided. The external MOS characteristics depend on the model and are subject to dispersion; therefore a fixed dead zone is not feasible without degrading the performance with a very conservative design. To overcome this problem a self-adapting dead zone has been exploited: before turning ON a MOS the complementary MOS's gate turning OFF is checked through a sensing path.
The dead zone management is very useful for the reduction of the switching noise, which affects the PWM output and the supply line. In fact it is possible to slow down the gate driving in order to slow down the drain current.

5. Experimental result

The chip is fabricated by using a 0.6 µm BCD (Bipolar, CMOS, DMOS) single-poly, triple-metal technology. The die size is 25 mm^2. Inside the chip some extra functions are implemented:

- Programmable digital clip-detector (@ THD = 1 %, 2 %, 5 % and 10 %)
- Internal thermal protection with thermal proximity output
- External thermal protection (NTC) with external thermal proximity output
- Short circuit protection
- Stereo / bridge operation selection pin
- Channel selection pin (bridge case)

Fig. 6 shows the die micrograph, where the digital block is a 26-kgate equivalent and its area amounts to about 9 mm^2.

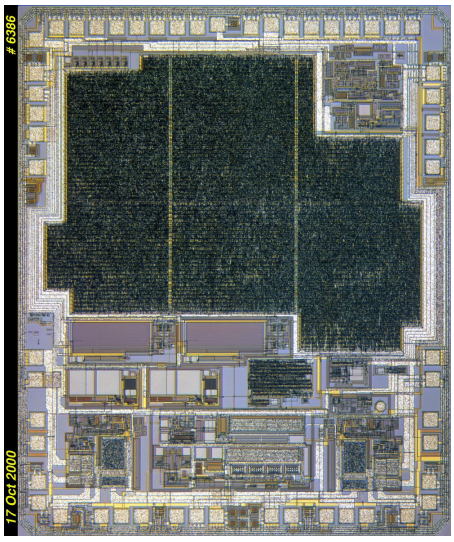

Figure 6. Die micrograph

In the measurement setup, an Audio Precision System One provides an AES/EBU audio signal, and a ST-Microelectronics STA120 chip converts this signal into a I^2S format and generates the 256 f_s master clock, which is subject to a time jitter of ≈ 300 ps rms.

Fig. 7 shows the result of an 8192-point FFT performed on the output signal delivered to a 4 Ω load, resulting from an applied input tone of 1 kHz 60 dBr, sampled at 44.1 kHz and quantized on 24 bits.
Fig. 8 shows the THD+N vs. output power in the same conditions, while Fig. 9 reports the efficiency curve.
The system could also drive a 2 Ω load suppling up to 500 W in bridge mode. The distortion for this configuration is shown in Fig. 10.
Table 1 gives an overview of the measurements performed on the chip loaded with a 4 Ω speaker, without additional filters.

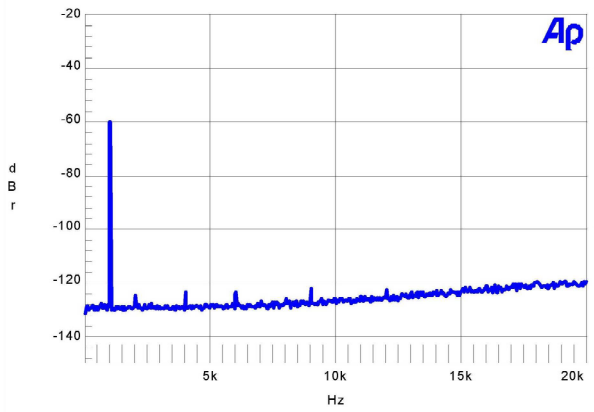

Figure 7. FFT(16348pt) @ Vs = +/- 25 V, Rload=4Ω

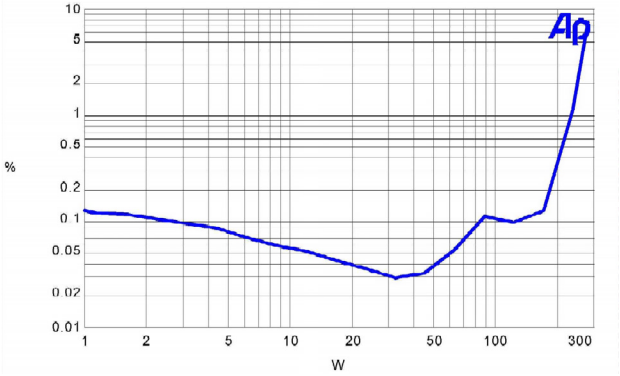

Figure 8. THD+N @ Vs = +/- 25 V, Rload = 4 Ω

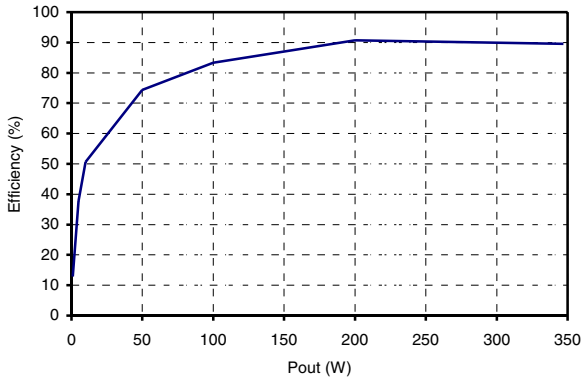

Figure 9. Efficiency @ Vs = +/- 25 V, Rload = 4 Ω

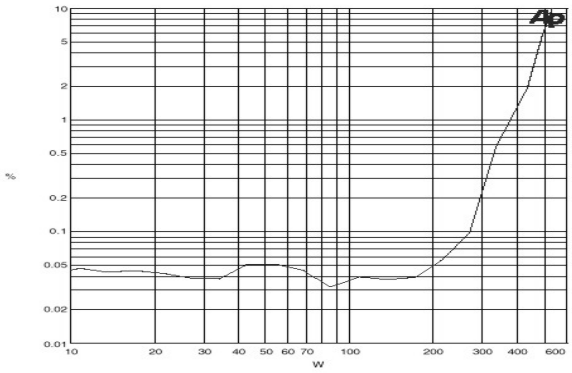

Figure 10. THD @ Vs = +/- 25 V, Rload = 2 Ω

Table 1. Main electrical parameters
Test conditions: voltage supply = +25 / -25 V, Rload = 4 Ω, f = 1 kHz, T = 25 deg.C

Parameters	Test Condition	Typ
Pout	THD=1% single ended	70 W
Pout	THD=1% bridge mode	250 W
Output Noise	"A" weighted, bridge mode	300 µV
THD+Noise	Pout 50 W	0.04 %
Dynamic Range	"A" weighted, bridge mode	96 dB
Efficiency	Pout=250W, bridge mode	90 %
Power Dissipation	Pout = 25W, bridge mode IC+Power Transistors	5 W
Die size	25 mm^2	
Package	HiQuad 64 pin	

6. References

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