A Low-Voltage Fully-Monolithic ΔΣ-Based Class-D Audio Amplifier

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Abstract

This paper presents a single-chip digital audio amplifier based on a delta-sigma (ΔΣ) modulator and a power-efficient switching (class-D) output-stage without intermediate filtering. Fabricated in a 0.18-μm standard digital CMOS process, this audio amplifier can operate from a single power-supply of 1.8V down to 1V, without significant change in performance. It has a measured total-harmonic-distortion (THD) at the speaker terminals of less than 0.07%, with a dynamic range (DR) of 85dB. An efficiency of 76% can be achieved with a 4.3-Ω speaker. The maximum output power is 350mW (rms) from a single 1.8-V power-supply, and the stand-by power consumption is only 7.5mW (load connected). This work demonstrates the feasibility of implementing class-D amplifiers with a high-end audio performance in low-voltage environments.

1. Introduction

As audio is increasingly derived from digital sources, the motivation to find a digital alternative to analog power-amplification is gaining more attention. Typically, the digital audio-data at the input of the power amplifier is a pulse-code-modulated (PCM) signal (as in a CD player, for example). It has, until recently, been necessary to convert the PCM audio-data to an analog signal in order to perform the power amplification. This approach has a low overall power-efficiency and usually comprises two chips with the digital-to-analog converter (DAC) and the amplifier implemented in different technologies (Figure 1).

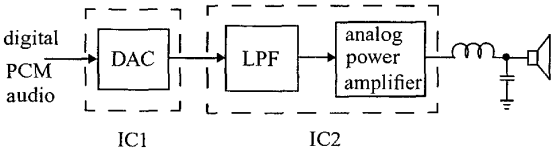

Figure 1: Conventional method for audio reproduction from a digital source

Several attempts have been made to implement a power amplifier capable of directly coupling to a digital source, thereby eliminating the need for first converting the digital audio-signal to analog [1-3]. Such digital amplifier (Figure 2) performs power amplification directly from the PCM digital audio-data and uses a class-D output stage for improved power efficiency. In contrast to class-AB amplifiers, class-D systems have a switching output stage whose transistors are always turned fully on or fully off, thereby achieving a high power efficiency (ideally 100%).

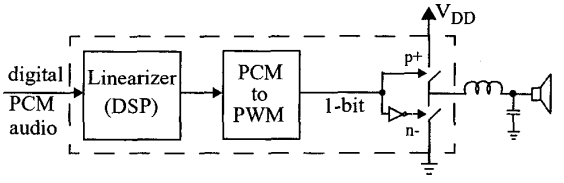

Figure 2: Typical digital amplifier architecture

In a class-D amplifier, the audio signal is converted into a high-frequency pulse-width-modulated (PWM) signal whose pulse width varies with the amplitude of the audio signal. The varying-width pulses switch the output transistors of the class-D output stage at a fixed frequency. A low-pass filter (LPF) then converts the output pulses into an amplified audio-signal that drives the speaker.

Direct PCM-to-PWM conversion (a process known as uniformly-sampled pulse-width-modulation or UPWM) introduces harmonic and non-harmonic distortion in the output spectrum of the amplifier [1,4]. A number of methods have been proposed to correct for the non-linearity of UPWM in order to minimize distortion in the audio band [1,3,4,5]. However, the proposed algorithms require heavy DSP computation and complex hardware to be implemented.

Alternatively to PWM algorithms, we employ ΔΣ modulation (as depicted in Figure 3) to generate a bitstream switching signal whose pulses have a fixed width and where the output signal is determined by the short-term pulse-density average. ΔΣ modulation offers a number of benefits over conventional PWM. Particularly attractive is its advantage of shaping the quantization noise and pushing it outside the audio band (where it can be filtered out by the LPF preceding the speaker), thereby resulting in an improved harmonic-distortion performance.

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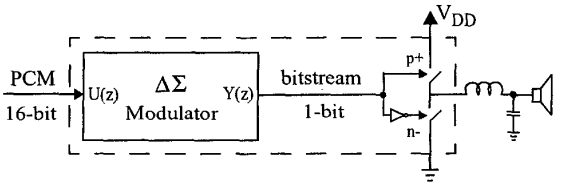


Figure 3: Proposed digital class-D amplifier architecture

In contrast to PWM-based digital amplifiers, a ΔΣ-based amplifier switches the transistors in the class-D output stage at a higher frequency, thereby dissipating more power. This is why PWM has been historically preferred. However, with the high-speed of modern technologies and when operating from low supply-voltages, this may no longer be an issue.

This paper is structured as follows: the digital ΔΣ modulator of the proposed class-D audio amplifier is described in Section 2, its class-D output stage is presented in Section 3, while its full integration is discussed in Section 4. The proposed class-D audio amplifier was fabricated in a 1.8-V 0.18-μm CMOS process and its measured performance is reported in Section 5.

2. ΔΣ Modulator

The ΔΣ modulator in Figure 3 is realized using the 3rd-order topology shown in Figure 4 and whose noise transfer function is given by:

$$NTF = \frac{(z-1)^3 + b_3\delta z(z-1)}{z^3 - (k_1 - b_3\delta)z^2 + (k_2 - b_3\delta)z - (1-a_2)} \quad (1)$$

where $k_1 = 3 - a_1b_3 - a_2$, $k_2 = 3 - a_1b_3 - 2a_2 + b_1b_2b_3$, and δ is the coefficient of the resonator feedback. Single-bit quantization is used to simplify the post-processing of the modulator's output signal while achieving a low harmonic-distortion.

To guarantee stability, the loop-filter coefficients must be chosen such that |NTF| < 1.5 over all frequencies. Furthermore, to reduce the digital hardware complexity, these coefficients must have a power-of-two value, which can be readily implemented using only adders and fixed-shift units (no multipliers are needed). Accordingly, the modulator was optimized to achieve the desired resolution (>16 bits for audio) at a low clock frequency of 5.6 MHz. The corresponding loop-filter coefficient values are given in Table 1.

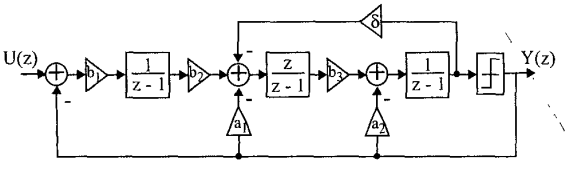


Figure 4: 3rd-order single-bit ΔΣ modulator

Table 1. Coefficient values of the ΔΣ modulator

$a_1=2^{-2}$	$b_1=2^{-2}$	$b_3=2^{-1}$
$a_2=2^{-1}$	$b_2=2^{-2}$	$\delta=2^{-13}$

The ΔΣ modulator was synthesized using digital 0.18-μm CMOS standard cells, and both behavioral and gate-level simulations were performed to verify the correct functionality of the system. Floor planning and routing was completed using specialized tools and some nets were manually routed to ease subsequent layout tasks.

3. Class-D Output-Stage

The class-D output stage (the output switches in Figure 3) is implemented using a bridge-tied-load (BTL) differential-drive configuration, as shown in Figure 5. The BTL configuration (or H-bridge) effectively doubles the voltage swing across the load (speaker). Furthermore, in low voltage applications, CMOS transistors can be used instead of conventional DMOS devices to realize cheaper monolithic H-bridges.

The discontinuous mode of operation of a class-D output stage results in a theoretical power efficiency of 100% when an ideal switching characteristic is assumed. In practice, however, the combination of switching and conduction losses sets an upper bound on the amplifier's power efficiency.

In a CMOS inverter, the main power dissipation mechanisms are due to:

1) the charging and discharging of the load capacitance:

$$P_c = f_c C_L V_{DD}^2 \quad (2)$$

where f_c is the average switching frequency and C_L represents the total load capacitance.

2) the direct-path (short-circuit) current when the NMOS and PMOS devices are simultaneously on during the input-signal transitions:

$$P_s = I_{mean} V_{DD} \quad (3)$$

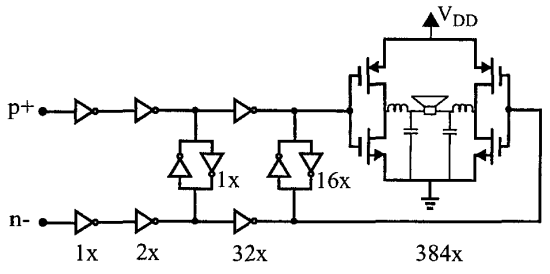
where I_{mean} is the mean value of the short-circuit current.

3) the on-resistance of the transistors:

$$P_r = \frac{1}{T}\int_0^T i_L(t)^2 R_{ON} dt \quad (4)$$

where $i_L(t)$ is the instantaneous load current and R_{ON} is the on-resistance of the transistors.

The static power dissipation P_r due to the transistors' on-resistance is ignored in digital-circuit analysis because the load impedance of these circuits is mainly capacitive. However, the load of the output inverters in an audio amplifier is considerably small (typically 4 to 36Ω). Therefore, this static power dissipation P_r (rather than the total dynamic power dissipation $P_c + P_s$) becomes the dominant factor in limiting the overall power efficiency.



Unit-size inverter dimensions:

W_p	13μm
W_n	5μm

Figure 5: Class-D output-stage circuit

Accordingly, the size of the transistors in the output switching stage is determined by the required on-resistance to meet the power efficiency specifications. For efficiencies in the order of 80%, the W/L ratio of these output transistors must be very large.

Due to the large width of the output transistors, a fully-differential multiple-stage buffer architecture was designed to drive the H-bridge (Figure 5). When designing such output-stage circuit, it is critical to ensure that the signals in each branch of the differential path have equal rise and fall times and, hence, reach the switching threshold-voltage of the inverters ($V_M=V_{DD}/2$) at exactly the same instant. This guarantees that, when one side of the H-bridge is pulling high, the other side is pulling low, and vice versa. If this condition is not properly met, both sides of the H-bridge will be pulling in the same direction during part of the switching transition, thereby resulting in a crossover-type distortion. Furthermore, fast signal transitions (small rise/fall times) is desirable as it helps reducing the short-circuit power dissipation P_s of the inverters.

In order to meet the requisites described above, weak cross-coupled inverters are inserted between the two differential lines of the output stage, as shown in Figure 5. The feed-forward provided by the cross-coupled inverters helps minimizing the signal skew. Simulations show that the differential signals are well matched (crossing each other at the switching threshold V_M and having a rise/fall time of less than 1ns) and the circuit is very robust against temperature and process variations.

The final design of the output stage is presented in Figure 5. A balanced LC-type differential LPF is connected between the H-bridge outputs and the speaker. A mixed-signal model of the entire audio-amplifier, including the effect of parasitics due to the pads, bondwires, and package was simulated in order to perform the final optimizations and evaluate the functionality of the full system.

4. Implementation

Due to the extremely large W/L ratio of the transistors in the H-bridge, the layout of the class-D output stage involves a number of design challenges. Some layout methodologies have been previously proposed [6]. Since the matching of the output transistors is critical to avoid introducing harmonic distortion, a common-centroid layout technique is used. With this approach, the output devices are constructed from interdigitated unit-sized transistors to help match the process errors caused by linear gradient effects across the microcircuit. To minimize the parasitic series impedance of the bondwires, several pins are used for the amplifier output signals. Furthermore, large on-chip bypass capacitors are included to source extra switching current and smooth the supply voltage.

The layout of the output-stage circuit and that of the digital ΔΣ modulator are integrated together and implemented in a 0.18-μm CMOS process. The chip micrograph is shown in Figure 6. The chip area is 3mm x 2mm. However, this design is severely pad-limited and the total active area is less than $0.3mm^2$. An 80-pin ceramic-flat-pack (CFP) was used for packaging the chip.

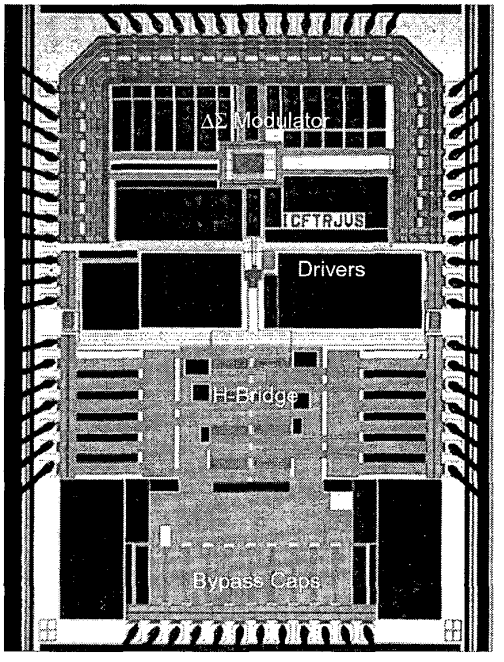


Figure 6: Chip microphotograph

5. Experimental Results

The following measurements were obtained in conformity with the "Audio Engineering Society standard method for digital audio engineering" [7]. A summary of the measurements characterizing the amplifier for various load impedances at a 1.8-V power-supply voltage is given in Table 2.

Table 2. Summary of measured performance at 1.8-V power-supply voltage

Load impedance	4.3Ω	8.2Ω	36Ω
THD	0.07%	0.07%	0.07%
SNR	74dB	77dB	71dB
Power into load (max)	350mW	200mW	80mW
Efficiency	76%	66%	79%

Figure 7 shows the measured output power spectrum of the amplifier when operating from a single 1-V or a single 1.8-V power supply. Accordingly, the amplifier can be powered from a supply as low as 1V without significant change in performance. A measured dynamic range (DR) of 85dB is achieved when driving a 4.3-Ω load from a 1-V power-supply.

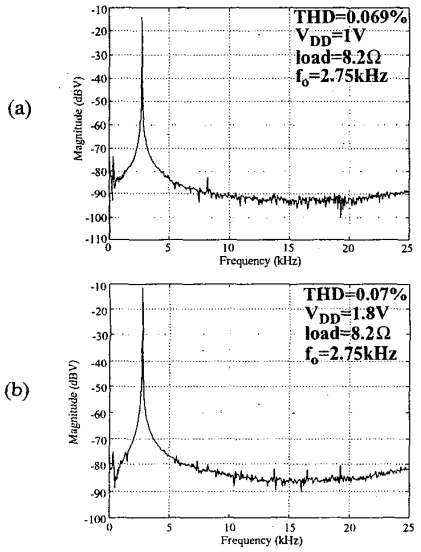


Figure 7: Measured power spectrum with an 8.2-Ω load when operating from: (a) 1-V supply voltage; (b) 1.8-V supply voltage.

Figure 8 shows the measured total harmonic distortion (THD) of the audio amplifier versus the output power for an input-signal of 2.75 kHz. Therefrom, the amplifier features a THD performance which is almost independent of the output power.

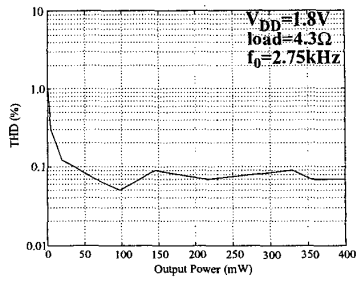


Figure 8: THD vs. Output power

6. Conclusion

This paper presented the design and experimental verification of a fully-integrated digital audio amplifier fabricated in a 0.18-μm standard digital CMOS process. This research demonstrates the feasibility of implementing a fast-switching class-D amplifier for low-voltage low-power applications with high efficiency. The use of direct ΔΣ modulation, instead of the traditional PWM mapping scheme, enables high-quality audio without the complexity of the hardware-intensive linearization algorithms. Furthermore, as the prototype was successfully tested at 1-V power-supply voltage, this circuit demonstrates enormous potential for a variety of wireless applications.

7. Acknowledgment

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