Realization of Digital Audio Amplifier Using Zero-Voltage-Switched PWM Power Converter

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Abstract—This paper presents a simple methodology to convert a hard-switched pulse-width-modulated (PWM) H-bridge converter used in a classical digital audio amplifier into a zero-voltage-switching (ZVS) converter. The ZVS is simply achieved by connecting an L-C series branch across the converter output. ZVS occurs during the dead time interval of the PWM signals, giving an effective improvement in the conversion efficiency, output frequency spectrum, and total harmonic distortion. A simplified design procedure is provided for choosing the value of the components. A prototype digital amplifier with an output power of 20 W and switching frequency of 705.6 kHz has been implemented. Experimental results are presented and favorably verified with theoretical predictions.

Index Terms—Pulse-width-modulated converter, total harmonic distortion, zero-voltage-switching.

I. INTRODUCTION

CONVENTIONAL digital audio playback system involves two main processes: the conversion of digital audio data to a low-level analog audio signal using a high-precision digital-to-analog converter (DAC) and the amplification of the analog signal using an analog power amplifier, such as Class A, Class B, and Class AB amplifiers. Since the early 1980’s, many researchers have been devoted to developing different types of digital amplifiers that perform power amplification directly from the digital audio data, e.g., [1]. This kind of amplifier is generally called a digital power amplifier and it has two main features: the elimination of the digital to low-level analog signal conversion and the improvement of the amplification efficiency using a Class D amplifier.

The most common approach to realize a digital power amplifier is to convert the pulse-code-modulated (PCM) digital audio data, as obtained from a compact disc (CD), into its corresponding PWM signal which is then applied to a PWM H-bridge converter. The loudspeaker is connected to the converter output via a low-pass filter, as shown in Fig. 1. In order to achieve the high-fidelity requirement, it is necessary to perform high-resolution PCM-to-PWM conversion. For the 16-bit audio data and 44.1-kHz sampling frequency used in the CD, the resolution of the PWM signal is $1/(44.1 \times 10^3 \times 2^{16}) = 346$ ps, which is extremely difficult to achieve even for low-power applications. A viable solution to solve this problem is to reduce the bit length of the digital audio data, such as in the method of direct truncation. However, this simple approach will theoretically cause a 6-dB reduction in signal to quantization noise ratio for truncating every one bit from the digital data.

A more sophisticated approach to achieve low quantization noise with short bit length is to apply oversampling and noise shaping to the PCM digital audio data [2], [3]. For example, the one-bit DAC chip that uses an oversampling ratio of 256 to convert 16-bit PCM data to a one-bit output for audio application is commercially available and widely used in CD players. The one-bit output can be considered as a special class of the PWM signal with a switching frequency of $256 \times 44.1$ kHz = 11.3 MHz. For low-power applications, such as the DAC IC’s, the implementation is feasible with such a high switching frequency. However, it is practically difficult to implement in high-power applications due to the finite turn-on and turn-off times of the switching devices. To make the digital power amplifier realizable, the oversampling ratio should be kept to a small and practical figure, such as a ratio of 16 that is used in the prototype described in this paper.

The implementation of a digital power amplifier is composed of two main stages. The first stage is to use an oversampling filter and noise shaper to reduce the 16-bit PCM data to a PWM signal with eight-bit resolution and high signal-to-noise ratio. The second stage is to use an efficient PWM converter to provide an audio output with high linearity and low total harmonic distortion (THD). With the consideration of the converter operation, a short dead time is commonly added to the PWM signal in order to avoid dead short of the supply through the upper and lower switching devices. However, the dead-time is known to be one of the major sources of harmonic distortion [4]. This paper presents a simple methodology to convert the hard-switched PWM H converter used in a classical digital power amplifier into a ZVS converter [5], [6] by simply connecting a series L-C branch across the converter output. ZVS occurs during the dead time period of the driving PWM signals, giving an effective improvement in the conversion efficiency, output frequency spectrum, and total harmonic distortion. In addition, the use of ZVS can effectively suppress the electromagnetic interference and minimize the switching losses [7].

The principles of operation and mathematical analysis of the proposed converter are given in Section II. Section III presents a simplified design procedure for choosing the component values.
of the \( L-C \) branch. Section IV illustrates the procedures of designing a 20 W prototype digital power amplifier operated with an oversampling ratio of 16. Experimental results are presented in Section V and the conclusions follow in Section VI.

II. PRINCIPLES OF OPERATION AND MATHEMATICAL ANALYSIS

Fig. 1 shows the circuit configuration of a hard-switched PWM \( H \)-bridge converter used in a classical digital power amplifier [1]. The load \( R_o \) (i.e., the loudspeaker) is connected to the converter output via a low-pass filter for suppressing the high-frequency components in the converter output \( v_{AB} \) and voltage across the nodes \( A \) and \( B \). In order to avoid short circuit of the dc supply through the upper and lower switches, for example \( S_1 \) and \( S_2 \), a short dead time \( t_{\text{dead}} \) is generally added at the rising edge of each gate signal. However, the introduction of this dead time can cause harmonic distortion to the converter output [4]. On the other hand, it is well known that the switching loss of the hard-switched converters will also be increased as the switching frequency increases [8]. This effect will then limit the choice of the switching frequency and, hence, the oversampling ratio.

With the above considerations, this paper presents a simple approach to modify the hard-switched PWM \( H \)-bridge converter to a ZVS one and consequently improve the waveform of \( v_{AB} \). As shown in Fig. 2(a), the modification is simply achieved by adding an inductor \( L_r \) and a capacitor \( C_r \), which are connected in series across nodes \( A \) and \( B \). During the dead time period \( L_r \), \( C_{S1} \), \( C_{S2} \), \( C_{S3} \), and \( C_{S4} \) form resonant paths and \( C_r \) acts as a temporary dc source with a value equal to the average output voltage \( V_o \). After low-pass filtering \( v_{AB} \), the average current through \( L_1 \) is approximately equal to the average output current \( I_o \) and can be considered to be constant within a switching cycle. Thus, a simplified equivalent circuit for illustrating the operation is shown in Fig. 2(b). Without loss of generality, it is assumed that the average voltage at node \( A \) is higher than that of node \( B \). The gate signals and the theoretical voltage and current waveforms of the converter are shown in Fig. 3. The topological operation of the converter is shown in Fig. 4. In order to simplify the mathematical analysis, the following assumptions have been made.

i) The circuit is under steady-state condition.

ii) All semiconductor switches have zero on-state resistance and infinite off-state resistance. Each switch has a finite parasitic capacitance \( C_{S1} \), \( C_{S2} \), \( C_{S3} \), and \( C_{S4} \), respectively, and they are all assumed to be equal to \( C_S \).

iii) All reactive elements are lossless.

iv) \( t_{\text{dead}} \) is very short as compared with the switching period \( T_S \) and can be neglected in the calculations. For example, the dead time used in the prototype digital power amplifier illustrated in Section IV is only 4.3% of the switching period.

v) The voltage across \( C_r \) is constant within \( T_S \).

A. Derivations of the Average Output Voltage and Current

As the switching frequency is substantially higher than the audio frequency, the duty cycle of the switches and the average value of \( v_{AB} \) (denoted by \( V_{AB} \)) are slow varying and of the same frequency as the audio signal. \( V_{AB} \) is equal to the average output voltage \( V_o \) across \( R_o \). With assumption iv), if \( D \) denotes the duty cycle of \( S_1 \) and \( S_3 \) (also of \( D_1 \) and \( D_3 \)) for a switching period \( T_S \), the duty cycle of \( S_2 \) and \( S_4 \) (also of \( D_2 \) and \( D_4 \)) is then equal to \((1-D)\). The values of \( V_o \) and \( I_o \) can be shown to be

\[
V_{AB} = V_o = \frac{V_{CC} \cdot D \cdot T_S + (-V_{CC})(1-D)T_S}{T_S} = \frac{V_{CC}(2D-1)}{T_S} \tag{1}
\]

\[
I_o = \frac{V_o}{R_o} = \frac{V_{CC}(2D-1)}{R_o} \tag{2}
\]

where \( D \approx (t_2 - t_0)/T_S \) since \( t_{\text{dead}} \ll T_S \).
B. Stages of Operation

As shown in Fig. 4, starting from the conduction of $D_2$ and $D_3$, there are totally six stages in one switching cycle. The operation of each stage is described as follows.

Stage 1—[$t_0$, $t_1$] [Fig. 4(a)]: After Stage 6, $D_2$ and $D_3$ start to conduct. Within this time interval, gate signals to $S_2$ and $S_4$ can be applied to achieve the zero-voltage condition in the next stage. At this stage, the voltages across $C_{S2}$ and $C_{S4}$ are equal to zero, while the voltages across $C_{S1}$ and $C_{S3}$ are equal to $V_{cc}$. The resonant inductor current $i_r$ is given by

$$i_r(t) = \frac{V_{cc} - V_o}{L_r} + i_r(t_0).$$

(3)

This stage ends when $i_r$ equals $-I_o$ and, consequently, $D_2$ and $D_3$ stop conduction.

Stage 2—[$t_1$, $t_2$] [Fig. 4(b)]: $S_1$ and $S_3$ start to conduct. $i_r$ will continue to increase linearly from $-I_o$ until $S_1$ and $S_3$ are turned off at $t_2$ with ZVS. Within this stage, $i_r$ is given by

$$i_r(t) = (t - t_1) \frac{V_{cc} - V_o}{L_r} - I_o.$$

(4)

Stage 3—[$t_2$, $t_3$] [Fig. 4(c)]: After $S_1$ and $S_3$ are turned off with ZVS, $C_{S1}$, $C_{S3}$, $C_{S2}$, $C_{S4}$, and $L_r$ form resonant paths in this stage. $C_{S1}$ and $C_{S3}$ are charging while $C_{S2}$ and $C_{S4}$ are discharging. $i_r$ and the voltage across the parasitic capacitors (i.e., $v_{cS1}$, $v_{cS2}$, $v_{cS3}$, and $v_{cS4}$) is given by

$$i_r(t) = -I_o [1 - \cos (\omega (t - t_2))] + 2V_{cc}(1 - D) \omega C_s \sin \omega (t - t_2) + i_r(t_2) \cos \omega (t - t_2)$$

(5a)

$$v_{cS1}(t) = v_{cS2}(t) = V_{cc}(1 - D) [1 - \cos \omega (t - t_2)] + \frac{1}{2 \omega C_s} \left[ V_{cc}(2D - 1) + i_r(t_2) \right] \sin \omega (t - t_2)$$

(5b)

$$v_{cS2}(t) = v_{cS1}(t) = V_{cc} - v_{cS1}(t).$$

(5c)

where $\omega = 1/\sqrt{L_r C_s}$. This stage ends when the voltages across $C_{S2}$ and $C_{S4}$ become zero and the voltages across $C_{S1}$ and $C_{S3}$ reach $V_{cc}$.

Stage 4—[$t_3$, $t_4$] [Fig. 4(d)]: $D_2$ and $D_3$ start to conduct. Similar to Stage 1, the expression of $i_r$ is given by

$$i_r(t) = i_r(t_3) - \frac{V_{cc} + V_o}{L_r} (t - t_3).$$

(6)

During this time interval, gate signals to $S_2$ and $S_4$ can be applied since the drain-source voltages across these switches are zero, providing ZVS condition for $S_2$ and $S_4$. This stage ends when $i_r$ equals $-I_o$.

Stage 5—[$t_5$, $t_6$] [Fig. 4(e)]: This stage is similar to Stage 2, where $S_2$ and $S_4$ start to conduct. $i_r$ continues to decrease linearly until $S_2$ and $S_4$ are turned off with ZVS. $i_r$ is given by

$$i_r(t) = -I_o - \frac{V_{cc} + V_o}{L_r} (t - t_4).$$

(7)

Stage 6—[$t_6$, $t_7$] [Fig. 4(f)]: This stage is similar to Stage 3, where $C_{S1}$, $C_{S3}$, $C_{S2}$, $C_{S4}$, and $L_r$ form resonant paths. $C_{S1}$ and $C_{S3}$ are discharging while $C_{S2}$ and $C_{S4}$ are charging. $i_r$ and the voltage across the parasitic capacitors is given by

$$i_r(t) = -I_o [1 - \cos (\omega (t - t_5))] - 2V_{cc}D \omega C_s \sin \omega (t - t_5) + i_r(t_5) \cos \omega (t - t_5)$$

(8a)

$$v_{cS1}(t) = v_{cS2}(t) = V_{cc}D [1 - \cos \omega (t - t_5)] - \frac{1}{2 \omega C_s} \left[ V_{cc}(2D - 1) + i_r(t_5) \right] \sin \omega (t - t_5)$$

(8b)

$$v_{cS3}(t) = v_{cS4}(t) = V_{cc} - v_{cS2}(t).$$

(8c)

This stage ends when the voltages across $C_{S1}$ and $C_{S3}$ are equal to zero and the voltages across $C_{S2}$ and $C_{S4}$ are equal to $V_{cc}$. This completes the operation in one switching cycle and the switching sequence returns to Stage 1.

By observing the switch voltage $v_{S1}$ (drain-source voltage) and switch current $i_{S1}$ in Fig. 3, all switches are ZVS. Moreover, $v_{AB}$ closely resembles the ideal PWM signal. Experimental results given in Section V also show that the converter with ZVS gives lower THD than that without ZVS.

As the voltage across $C_r$ is constant within $T_S$, the average capacitor current or the average value of $i_r$ equals zero. As shown in Fig. 3, if the dead time is negligible, DEF and FGH
can be approximated by two similar triangles with equal area. Therefore

\[ i_r(t_2) = -i_r(t_3) \quad \text{and} \quad D\bar{F} = FF = \frac{T_S}{2}. \]  

(9)

Based on (3) and (4), it can be shown that

\[ i_r(t_2) = \frac{D(1 - D)T_S}{L_r} V_{CC}. \]  

(10)

C. Open-Loop Low-Frequency Transfer Characteristics of the Converter

As shown in (1), \( V_o \) depends on \( V_{CC} \) for a fixed duty cycle operation. The low-frequency input-to-output transfer characteristics [i.e., \( \frac{V_o(s)}{V_{CC}(s)} \)] can be shown to be

\[ \frac{V_o(s)}{V_{CC}(s)} = 2D. \]  

(11)

In normal operation, \( D \) is an explicit parameter for controlling \( V_o \) if \( V_{CC} \) is fixed. The low-frequency control-to-output transfer function, i.e., \( \frac{V_o(s)}{D(s)} \), can be determined by considering the transfer functions of \( \frac{v_{AB}(s)}{D(s)} \) and \( \frac{V_o(s)}{v_{AB}(s)} \), i.e.,

\[ \frac{V_o(s)}{D(s)} = \frac{v_{AB}(s)}{D(s)} \cdot \frac{V_o(s)}{v_{AB}(s)} = 2V_{CC} \cdot \frac{V_o(s)}{v_{AB}(s)}. \]  

(12)

where \( \frac{V_o(s)}{v_{AB}(s)} \) is the transfer function of the output low-pass filter. In order to suppress the high-frequency components appeared in \( v_{AB} \), a fourth-order low-pass filter [9] as shown in Fig. 2(a) is used and its transfer characteristics is given as shown in (13) at the bottom of this page.

As mentioned in Section I, the overall digital power amplifier consists of two units, including a PCM to PWM conversion unit and the proposed power converter unit. Since the proposed converter is operated in an open-loop manner and its stability of operation is ensured [10], the overall system stability of the digital power amplifier is therefore dependent on the PCM to PWM conversion unit. Since the conversion of PCM to PWM is a process of changing the data representation [11], the audio-band frequency spectrum of the output PWM signal is dependent on the type of the sampling technique. For the uniform sampling used in CD and with sufficient oversampling ratio and

\[ \frac{V_o(s)}{D(s)} = \frac{2V_{CC}}{L_1L_2C_1C_2} \cdot \frac{1}{s^4 + \frac{2}{R_oC_2} s^3 + \left( \frac{1}{L_1C_2} + \frac{1}{L_2C_2} + \frac{1}{L_2C_1} \right) s^2 + \frac{1}{R_o} \left( \frac{2}{L_1C_1C_2} + \frac{2}{L_2C_1C_2} \right) s + \frac{1}{L_1L_2C_1C_2}} \]  

(13)
noise shaping, the audio band frequency spectrum of the corresponding PWM signal can approximate to that of the original PCM digital audio signal. The overall system transfer characteristics can then be determined by (13), which is solely dependent on the values of the passive components \( L_1, L_2, C_1, \) and \( C_2 \).

D. Conversion Between the Modulation Index and the Duty Cycle

In normal operation, \( D \) varies according to the audio signal but in much lower frequency than the switching frequency. In order to give a measure of a sinusoidal output voltage with respect to the supply voltage, a modulation index \( M \) is defined as follows:

\[
M = \frac{V_{\text{max}}}{V_{\text{CC}}}
\]

where \( V_{\text{max}} \) is the maximum amplitude of \( v_o \). Hence, for a given \( M \), \( D \) varies between a minimum value \( D_{\text{min}} \) and a maximum value \( D_{\text{max}} \), i.e.,

\[
D_{\text{min}} = \frac{1}{2}(1 - M)
\]

and

\[
D_{\text{max}} = 1 - D_{\text{min}} = \frac{1}{2}(1 + M).
\]

III. SIMPLIFIED DESIGN PROCEDURE FOR CHOOSING THE VALUES OF \( L_R \) AND \( C_R \)

A. Upper and Lower Limits of \( L_r \)

To ensure ZVS, \( v_{C1} \) (or \( v_{C2} \)) must reach \( V_{\text{CC}} \) in Stage 3 operation before applying the driving signals to \( S_1 \) and \( S_2 \). Similarly, \( v_{C2} \) (or \( v_{C3} \)) must reach \( V_{\text{CC}} \) in Stage 6 operation before applying the driving signals to \( S_3 \) and \( S_4 \). Moreover, the duration of Stage 3 and Stage 6 must be less than \( t_{\text{lead}} \). For the Stage 3 operation, if \( \omega(t_3 - t_2) \) is chosen to be less than \( \pi/4 \) (i.e., \( \leq 55 \) ns), (5b) gives

\[
V_{\text{CC}}(1 - D)[1 - \cos(\pi/4)] + \frac{V_{\text{CC}}}{2\omega C_S} \left[ \frac{2D - 1}{R_o} + \frac{D(1 - D)T_S}{L_r} \right] \sin(\pi/4) \geq V_{\text{CC}}.
\]

Hence

\[
(2D - 1)L_r - 2R_o \psi \sqrt{L_r/C_S} + D(1 - D)T_S R_o \geq 0
\]

where

\[
\psi = \frac{D + (1 - D) \cos(\pi/4)}{\sin(\pi/4)}.
\]

Similarly, for Stage 6 operation, (8b) also gives the same expression as (17). It can be shown that the solution to (17) is given by

\[
L_r \leq \left[ \frac{\psi R_o \sqrt{C_S} - \sqrt{\psi^2 R_o^2 C_S + T_S R_o D(2D - 1)(D - 1)}}{2D - 1} \right]^2.
\]

On the other hand, the maximum switch current \( I_{\text{max}} \) will also limit the choices of value for \( L_r \) in Stages 2 and 5 operations, i.e.

\[
\left| i_r(t_2) \right| = \left| i_r(t_5) \right| \leq I_{\text{max}}.
\]

By substituting (10) into (19), it gives

\[
L_r \geq \frac{D(1 - D)T_S V_{\text{CC}}}{I_{\text{max}}^2}.
\]

The lower and upper limits of \( L_r \) are given by both (18) and (21) to ensure ZVS and acceptable current stress on the switches.

B. Upper and Lower Limits of \( C_r \)

As mentioned in Section II, the voltage across \( C_r \) approximates \( V_o \) and has small ripple voltage within a switching cycle. The time interval between \( D \) and \( F \) shown in Fig. 3 is the charging period of \( C_r \). If \( \Delta V_{C_r} \) represents the maximum allowable ripple voltage on \( C_r \), we have

\[
\Delta V_{C_r} \geq \frac{1}{C_r} \int_{t_0}^{T_s/2} i_r(t) dt \geq \frac{D(1 - D)T_s^2 V_{\text{CC}}}{4L_r C_r}.
\]

Hence, the lower and upper limits of \( C_r \) are governed by both (23) and (25).

IV. ILLUSTRATIVE EXAMPLE

A prototype digital power amplifier has been realized. The specifications are as follows:

1) supply voltage, \( V_{\text{CC}} = 30 \) V;
2) maximum AC output power, \( P_{\text{out}} = 20 \) W;
3) output loudspeaker resistance, \( R_o = 4 \) \( \Omega \);
4) maximum allowable switch current, \( I_{\text{max}} = 15 \) A;
5) switching frequency, \( f_s = 16 \times 44.1 \) kHz = 705.6 kHz \( \Rightarrow T_s = (1/f_s) = 1.417 \) \( \mu \)s;
6) dead time, \( t_{\text{dead}} = 60 \) ns \( \approx 4.3\% \) of \( T_s \);
7) maximum ripple voltage on \( C_r \), \( \Delta V_{C_r} = 500 \) mV.
The prototype amplifier consists of two main units, namely, a PCM to PWM converter and a ZVS H-bridge PWM converter. Each unit is briefly described in the following.

A. Design of the PCM to PWM Converter

A digital signal processing hardware platform based on DSP56002 has been built to perform real-time oversampling, noise shaping, and PCM to PWM conversion. The CPU clock frequency is 40 MHz. The 16-bit PCM digital audio data is directly decoded from the digital output of a CD player and is reduced to eight-bit length with the aid of digital interpolation filter and noise shaper. Due to the limited computational capability, the oversampling ratio of the interpolation filter is limited to 16 times (i.e., the switching frequency is 705.6 kHz) and the noise shaper is a second-order structure. The noise shaped eight-bit PCM audio data is then converted to a PWM output using a pulse width modulator chip AD9561. The PWM signal which will be applied to the gate driver circuit.

B. Design of the H-Bridge Converter

All MOSFET’s shown in Fig. 2(a) are IRF530. The diodes are the intrinsic body diodes and $C_S = 2000 \text{ pF}$. The four PWM signals are applied to their corresponding gate drivers DS0026 via optical isolators 74O16010. If the input signal is assumed to be sinusoidal, the peak value of the output signal $V_{o_{\text{max}}}$ can be determined by

$$P_{\text{out}} = \left( \frac{V_{o_{\text{max}}}}{R_o} \right)^2 \Rightarrow V_{o_{\text{max}}} = 12.65 \text{ V}. \quad (26)$$

Moreover, the maximum modulation index is given by

$$M = \frac{V_{o_{\text{max}}}}{V_{CC}} = \frac{12.65}{30} = 0.422$$

$$\Rightarrow D_{\text{min}} = \frac{1}{2} (1 - M) = 0.29$$

and

$$D_{\text{max}} = \frac{1}{2} (1 + M) = 0.71. \quad (27)$$

By substituting $D = D_{\text{max}}$ into (18) and using (21), we obtain the limits for $L_r$, i.e.,

$$3.22 \mu \text{H} \geq L_r \geq 0.7 \mu \text{H}. \quad (28)$$

An inductor of 2.5 $\mu$H is chosen for $L_r$ in the prototype amplifier.

The value of the capacitor $C_r$ can be chosen with the aid of (23) and (25). For $k = 5$ and $f_{\text{in}} = 20 \text{ kHz}$, we obtain the limits of $C_r$, i.e.,

$$5 \mu \text{F} \geq C_r \geq 2.48 \mu \text{F}. \quad (29)$$

A capacitor of 4.7 $\mu$F is chosen for $C_r$ in the prototype amplifier.

C. Design of the Output Low-Pass Filter

To suppress the high-frequency components in the converter output, a fourth-order low-pass filter given in (13) is used. The cutoff frequency of the filter is set to 20 kHz and the component values are: $L_1 = 16.4 \mu \text{H}$, $L_2 = 11.68 \mu \text{H}$, $C_1 = 4.4 \mu \text{F}$, and $C_2 = 1 \mu \text{F}$. The theoretical and experimental frequency characteristics of the low-pass filter is shown in Fig. 5. The experimental results are measured with the audio precision system one.

V. EXPERIMENTAL RESULTS

The experimental results given in this section are obtained with input signals taking from a testing CD (A-BEX) with standard tones. The results are measured with a constant output power of 20 W. The gate signals applied to $S_1$, $S_2$, $S_3$, and $S_4$, the waveforms of $v_{\text{AB}}$ and $i_r$ of the ZVS converter are measured with HP Infinium oscilloscope and shown in Fig. 6. These waveforms are consistent with the theoretical predictions, as shown in Fig. 3. The input and output voltage waveforms of the digital power amplifier for input signals of 1 and 20 kHz are shown in Fig. 7. The value of $M$ for this test is set to 0.4. Fig. 8 shows that the rms output voltage is linearly varied with $M$. Thus, the amplitude linearity characteristics of the digital power amplifier are confirmed. To verify the frequency response of the digital power amplifier, the measured magnitude and phase response...
curves are compared with the theoretical responses as shown in Fig. 5. It can be seen that the magnitude response is constant with nearly linear phase over the entire audio frequency band (i.e., from 20 Hz to 20 kHz).

With an input signal of 1 kHz and output power of 20 W, the frequency spectra of the digital power amplifier obtained with a hard-switched converter (without $L_C$) and a ZVS converter (with $L_C$) are shown in Fig. 9. It is clearly shown that the presence of $L_C$ can improve the harmonic distortion. The total-harmonic-distortion-plus-noise (THD+N) increases from 0.281% to 0.585% when the $L_C$ branch is removed. The THD+N for the entire audio band under different output power is shown in Fig. 10. The effect of improving the THD+N with the presence of $L_C$ is clearly demonstrated. It should be noted that the signal harmonics appeared in the output spectra are generated by the PCM to PWM converter AD9561. In principle, by observing the spectrum for an input signal above 10 kHz for which all signal harmonics will be outside the audio frequency band, the THD+N of this amplifier is just less than 0.1% if all the signal harmonics are suppressed and this should be achievable with the ASIC chip [11] specifically designed for this purpose.

One of the major advantage of using ZVS converter is to improve efficiency. With an input signal of 1 kHz, the overall efficiency of the amplifier for various output powers is shown in Fig. 11. As compared with the hard-switched converter, an average of 15% improvement in efficiency has been observed. In addition, the efficiency is shown to increase as the output power increases. A maximum of 82% efficiency has been recorded. On the other hand, the efficiency is shown to be fairly low for low output power and this is attributed to the conduction loss on the switches. Experimentally, it was found that the input power is about 2 W when $M$ equals zero and this can be considered as a constant power loss. Thus, for low power output, such a loss becomes significant and results in lower efficiency. On the contrary, the conduction loss becomes insignificant for high power output and the efficiency hence increases. In summary, the proposed digital amplifier is suitable for high power output which is the major objective of using the switching converter in high power audio amplification.

VI. CONCLUSION

The design of a digital power amplifier using zero-voltage-switched PWM $H$-bridge converter is presented. By simply adding a $L-C$ circuit across the converter output, a classical hard-switched converter becomes a ZVS one without the need
of modifying the gate signals. A simple design procedure for choosing the component values of the $L-C$ circuit is given. The control-to-output characteristics and the stability of operation have been discussed. Experimental results show that the ZVS converter not only improves the efficiency, but also gives better output frequency spectrum and total harmonic distortion. Further research will be dedicated to applying a similar ZVS technique in multilevel converter for achieving higher output power with lower harmonic distortion.

REFERENCES


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