A Topology Survey of Single-Stage Power Factor Corrector

with a Boost Type Input-Current-Shaper

Chongming Qiao and Keyue M. Smedley
Department of Electrical and Computer Engineering
University of California, Irvine. CA 92697
Tel: (949) 824-6710
Fax: (949) 824-3203
Email: smedley@ uci.edu

Abstract: A topological review of the single stage power factor correctted (PFC) rectifiers is presented in this paper. Most of reported single-stage PFC rectifiers cascade a boost-type converter with a forward or a flyback dc-dc converter so that input current shaping, isolation, and fast output voltage regulation are performed in one single stage. The cost and performance of a single-stage PFC converters depend greatly on how its input current shaper (ICS) and the dc-dc converter are integrated together. For the cascade connected single-stage PFC rectifiers, the energy storage capacitor is found in either series or parallel path of energy flow. The second group appears to represents the main stream. Therefore, the focus of this paper is on these group. It is found that many of these topologies can be implemented by combining a 2-terminal or 3–terminal boost ICS cell with dc-dc converter along with an energy storage capacitor in between. A general rule is observed that translates a 3-terminal ICS cell to a 2-terminal ICS cell using an additional winding from the transformer and vice versa. According to the translation rule, many of reported single-stage PFC topologies can be viewed as electrically equivalent to one another. Several new PFC converters were derived from some existing topologies using the translation rule.

I INTRODUCTION

Traditional diode rectifiers used in front of the electronic equipment draw pulsed current from the utility line, which deteriorates the line voltage, produce radiated and conducted electromagnetic interference, leads to poor utilization of the capacity of the power sources[1]. In compliance with IEC 1000-3-2 harmonic regulation, many power factor corrected ac-dc rectifiers have been proposed in recent years. For single-phase electronics applications, passive power filters, active one and two stage power factor correction (PFC) rectifiers are typical approaches used to achieve high power factor and low total-harmonic-distortion (THD). Passive power filters exhibit high efficiency and low cost, but they are bulky and heavy due to the size of the line frequency inductors and capacitors. The two-stage PFC approach uses an input current shaping converter in front of a dc-dc converter. The two converters are controlled independently to achieve high quality input current shaping and fast output voltage regulation. This method is known for its superior performance, such as high power factor, low input current harmonics, good hold-up time, optimized design of the dc-dc converter, but at the cost of additional semiconductor switches and control circuitry that may not be justified for lower power applications. In a single-stage PFC, input-current shaping, isolation, and fast output regulation are performed in a single stage. A single-stage PFC rectifier typically integrates an input current shaper and an isolated dc-dc converter with a shared switch and controller. The energy storage device in between serves as a buffer for frequency isolation between the ICS and the dc-dc converter as well as provides necessary hold up time. This method provides a compromise between the performance and cost. Comprehensive comparisons of the three approaches at manufacture cost and performance [2][3] have shown that the single-stage PFC is a cost-effective solution for low power applications (typical below 200watts).

For single stage PFC rectifiers, the performance measures, such as efficiency, hold up time, component count, component voltage and current stress, input current quality, etc., are largely dependent of the circuit topology. In recent years, the heat wave of searching for single stage PFC rectifiers has resulted in hundreds of literatures and countless topologies. This paper presents a topological study of the representative single phase PFC rectifiers. The intention of this study is to find a topological relationship among various rectifiers and to provide researchers a reference. In Section II, a topological review of single stage PFC rectifiers is given. Many single-stage PFC can be viewed as a combination of the dc-dc converter with a 2-terminal or 3-terminal ICS cell, which is described in Section III. Section IV presents the observed translation rule between 2-terminal or 3-terminal ICS cell. Applications of the observed translation rule are discussed in Section V. Finally, a conclusion is given in Section VI.

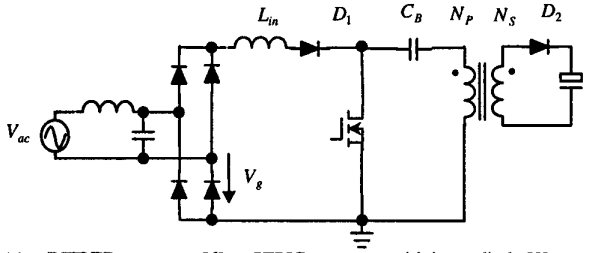
Resonant type of rectifiers and rectifiers for light ballast applications are not in the scope of this paper.

II REVIEW OF SINGLE STAGE PFC TOPOLOGIES

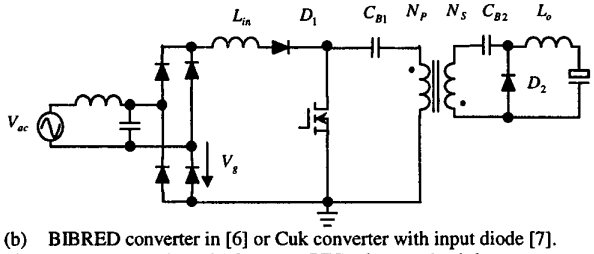
Concept for single-state PFC can be traced back to some early work presented in [4][5]. In article [4], a single power stage with dual outputs produces both the desired DC output and a boosting supply in series with the input. Without active control of the boost supply, a reasonably good input current shape results due to the natural gain

0-7803-5864-3/00/$10.00 © 2000 IEEE

characteristics of the boost resonant circuit. This circuit is original but the component count is high. Another way to realize single stage PFC is by cascading a boost ICS with a dc-dc converter using one switch as shown in [5]. Both pulse width modulation (PWM) and frequency modulation (FM) were applied in the control circuitry. The rectifier has very high power factor. However, the circuit suffers wide frequency variation and high voltage stress. Nevertheless, this circuit presents an early form of the single stage PFC method that integrates a boost ICS with a dc-dc converter in a cascade fashion. A very systematic synthesis of single stage PFC using cascade method was initiated in article [6] in 1992, in which some new PFC rectifiers, BIFRED and BIBRED, were resulted from integrating a boost input current shaper with a flyback or buck converter as shown in Fig. 1. The characteristic marker of these rectifiers is that the energy storage capacitor is in the series path of the energy flow. Synthesis of single stage PFC by inserting a diode in front of the Cuk and Sepic converters have resulted in the same topologies[7][8]. In BIFRED and BIBRED, the boost ICS operates in discontinuous conduction mode (DCM) to achieve automatic input current shaping, while the dc/dc converter operates in continuous conduction mode (CCM). The dc-bus capacitor voltage has a strong dependency on the output load. For universal input applications, it will suffer high voltage stress at light load. Articles [7][9] use frequency modulation method to keep the dc-bus voltage under control during light load. Article [8] shows a new operation mode that operates both the boost and the flyback in DCM, which has effectively reduced the dc-bus voltage and significantly improved the input current waveform.



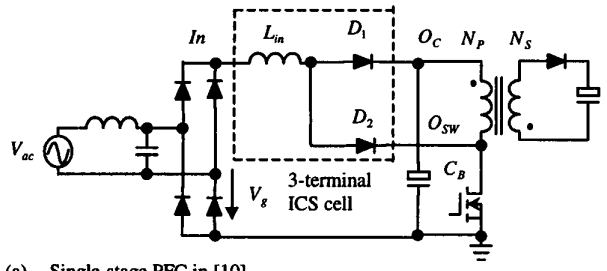
(a) BIFRED converter [6] or SEPIC converter with input diode [8].



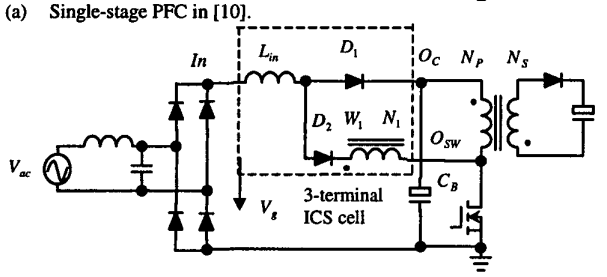
(b) BIBRED converter in [6] or Cuk converter with input diode [7].

Fig. 1. Representative single-stage PFC characterized by an energy storage capacitor in the series path of the energy flow.

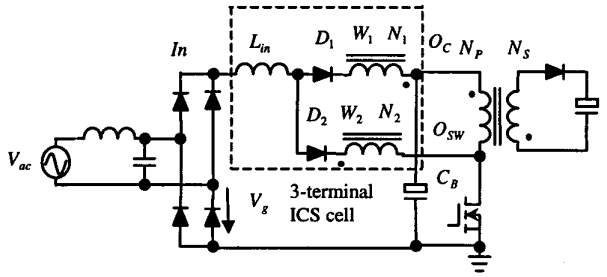
In 1994, a new family of single-stage PFC converter was synthesized in [10] that integrates a boost ICS with a dc/dc converter in such a way that the energy storage capacitor is in the parallel path of the energy flow as shown in Fig. 2 (a). In all the PFC converters shown in [10], the boost ICS operates in DCM to achieve automatic input current shaping, while the dc/dc converter may operate in either CCM or DCM. However, if the dc-dc converter is in CCM, the dc-bus capacitor voltage varies with the output load. For universal input applications, it will suffer high voltage stress at high input voltage and light load, which requires expensive capacitors and increases the switch voltage stress. This phenomena appears inherent to the rectifiers that cascade a boost ICS with dc-dc converter as shown in [5][6][10]. Switching frequency modulation methods were reported to alleviate the dc-bus voltage [11][12][13]. However, the switching frequency could span ten times over the whole load range in order to maintain the dc-bus voltage be low 450V, which is undesirable for the magnetic component design. Another way to suppress the dc bus voltage is to keep the dc/dc converter in DCM for the entire load range [14][15][16], because the dc-bus voltage becomes independent of the load in DCM. However, for low voltage applications, e.g. computer power supplies, CCM operated dc/dc converter is preferred, since it leads to lower conduction loss and smaller ripple. As a result, a compromise between the THD and the voltage stress was proposed in article [17] by negative magnetic feedback using an additional transformer winding during the switch on interval as shown in Fig. 2(b). Similar approaches were seen in [18]. Article [19] presents a very comprehensive study of the magnetic feedback phenomenon and design guideline. With this negative feedback, the conduction angle of the input current is reduced. The gained benefit is that the dc bus capacitor voltage V_{CB} may be maintained below 450V while the dc-dc converter is in CCM for heavy load, which warrants the use of low cost 450V electrolytic capacitors. A single-stage PFC method with double negative magnetic feedbacks (feedback during both switch on and off intervals) was proposed [20][21] as shown in Fig. 2 (c). This method can also keep the voltage V_{CB} below 450V. In addition it enables CCM operation of both the ICS and the dc-dc converter while the input harmonics are still within the range of Class D standard. In order to reduce the conduction loss and ripple in the input, several single-stage PFC rectifiers with CCM operated ICS were proposed recently as shown in Fig. 2 (d), (e) (f), (g). The converter in Fig. 2 (d) was derived from the charge bump concept [23] and the converters in Fig. 2 (e-g) are based on series insertion of a voltage source and a loss free resistor in between the diode bridge and the dc-dc converter [24]-[28]. Magnetic switch concept was introduced in [29]-[33], where the ICS usually contains one additional winding coupled to the transformer of dc/dc converter. Several examples are shown in Fig. 2 (h), (i), (j), where the input ICS cell in Fig. 2 (i) operates in CCM. Note that although the flyback dc/dc converter is shown in all approaches in Fig. 2, the discussion in this paper are applicable to forward and other topologies as well.



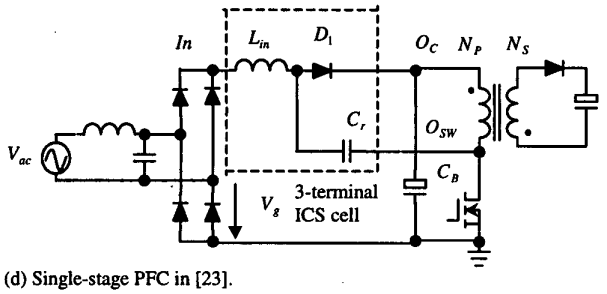
(a) Single-stage PFC in [10].



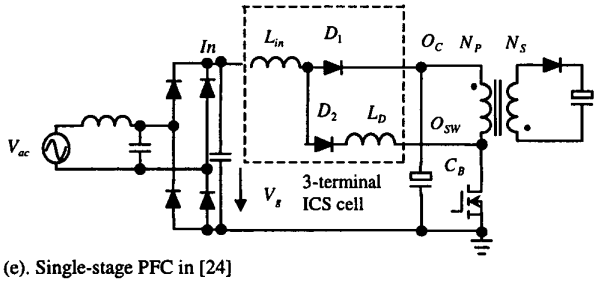
(b) Single-stage PFC in [17], $N_1 < N_p$.



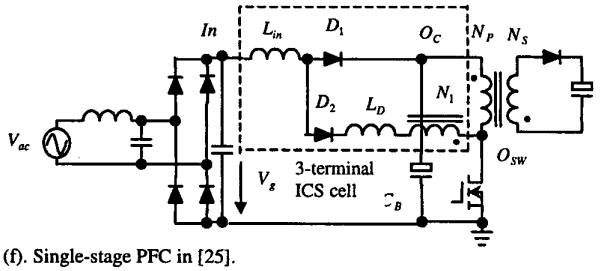
(c). Single-stage PFC in [20] [21][22], $N_1, N_2 \le N_p$



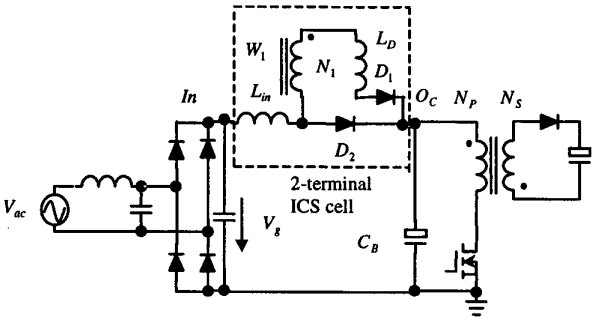
(d) Single-stage PFC in [23].



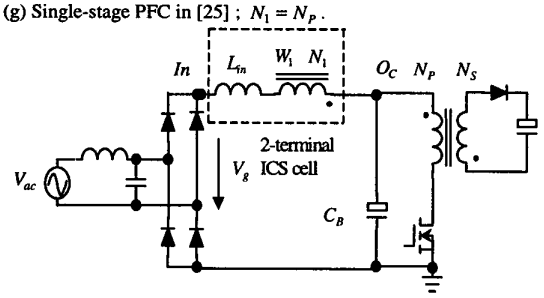
(e). Single-stage PFC in [24]



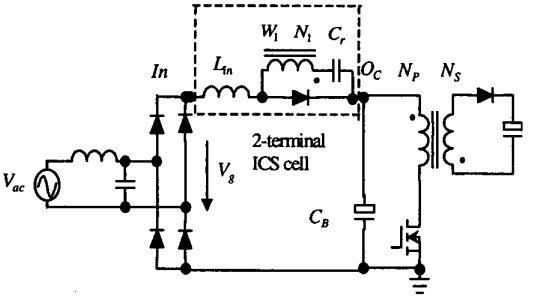
(f). Single-stage PFC in [25].



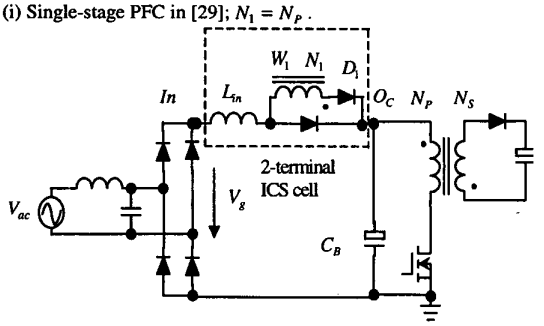
(g) Single-stage PFC in [25] ; $N_1 = N_P$.



(h) Single-stage PFC in [29]; $N_1 = N_P$.



(i) Single-stage PFC in [29]; $N_1 = N_P$.



(j) Single-stage PFC in [31]; $N_1 = N_P$.

Fig. 2. The representative single-stage PFC topologies characterized by connecting the energy storage capacitor in the series path of the energy flow.

Topologies variations are also found in many other forms. A parallel PFC concept was reported in [34], while three switch-states were used to provide two dimentional control for the PFC function and fast output regulation. The performance is commendable but the implementation is very complicated. In article [35][36], a flyback converter is used as ICS, which results in better input current waveform but higher current stress. An interesting method of combining a boost ICS with a forward converter with two energy storage capacitors was shown in [37]. With two capacitors, the spike due to the leakage inductance during switch turn off is subdued. Very good performance was demonstrated. Article [38] shows a new single stage PFC rectifier that uses an ac side inductor and additional two diodes to directly connect the ac voltage to the switch. This circuit has similar operational principle as the one proposed in [10], but with less conduction loss. The rectifier proposed in [16] uses a boost bridge rectifier that shares its switches with the following flyback dc-dc converter with the intention to increase the power level. Since both the boost bridge rectifier and the flyback converter operate in DCM, the conduction loss is high. In addition, this circuit may suffer high common mode noise. Article [39] presented a rectifier that integrates a boost ICS and a half bridge dc-dc converter. Synchronized rectifiers are used to achieve high efficiency for low voltage applications. Article [40] proposed a regenerative clamping circuit for single-stage PFC to reduce the turn-off losses and stress of the switch. In addition, the power factor is also improved. Article [41] reported a single stage high power factor converter using the Sheppard-Taylor topology. Two possible operation regimes are described. Compared to the usual boost-buck cascade operating in the first regime, the proposed converter has a wider operating range. When operating in the second regime, the modified boost stage has the ability of producing a harmonic free input current, unlike the standard boost PFC whose current always suffers a cusp distortion. A new parallel approach for single stage PFC was reported in [42][43][44][45] that employs an auxiliary dc/dc converter to supplement energy to the load when the direct power from the line is low. This method improves overall efficiency because only partial energy is processed twice. An additional switch is required. Extensive syntheses were performed in [46][47] that yielded many families of single stage PFC rectifiers based on dither effect [46] and partial energy processing [47]. These two papers present interesting teaching from the principle of synthesis as well as analysis to the implementation of the new circuits, thus are valuable to researchers in the power factor correction area.

III 2-TERMINAL AND 3-TERMINAL INPUT CURRENT SHAPER (ICS) CELL

From the above review of the single stage PFC rectifiers, it is noticed that the group of circuits shown in Fig 2, characterized by the energy storage capacitor in the parallel path of the energy flow, represents the main stream. The focus of this paper is thereby on the topological rules of this group of rectifiers. The 2 or 3 terminal concept shown in [48] is extended to study the ICS cells. In spite of different PFC realization mechanism, from topology point of view, the input current shaping circuits in Fig. 2 can be symbolized as 2 or 3-terminal cells as shown in Fig. 3. Each ICS cell contains an input inductor L_{in} and two branches. The "charge branch" is used to charge the input inductor when switch is on. The "discharge branch" is used to discharge the inductor and transfer the energy from input inductor to bulk capacitor or output when the switch is off. The branches are usually composed of diodes, capacitor, inductors, extra windings of the transformer or their combinations. Terminal In is connected to the input diode bridge; terminal O_C is connected to the dc-bus bulk capacitor C_B; and terminal O_{SW} is connected to the switch in dc-dc converter.

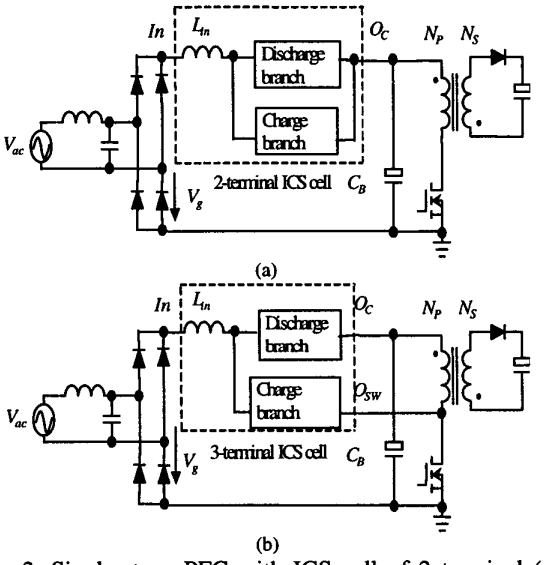


Fig. 3. Single-stage PFC with ICS cell of 2 terminal (a) and 3-terminal (b).

The 2-terminal ICS cell is inserted between the input diode bridge and dc bus capacitor. It contains one winding coupled to the transformer of dc/dc converter in the charge branch. When the switch is on, the voltage across the winding cancels the capacitor voltage, so that the inductor sees only the input voltage that charges the inductor. The input inductor is discharged through discharge branch when the switch is off. The topologies in Fig. 2 (g-j) are several examples of single-stage PFC with 2-terminal ICS cells.

In a 3-terminal ICS cell, the switch is connected in series with the charge branch. When the switch is on, the input inductor is charged through switch. Similar to the 2-terminal ICS cell, the inductor current is discharged through discharge branch. The ICS cells in topologies of Fig. 2 (a-f) belong to this group. Two examples of ICS cell are illustrated in Fig. 4.

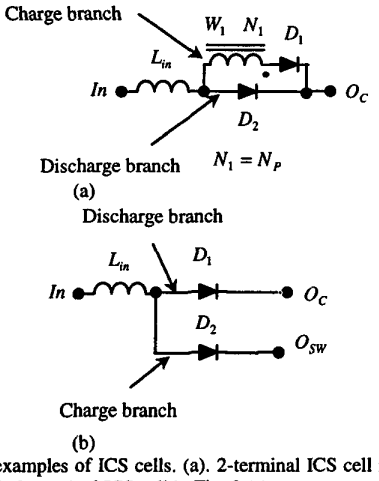


Fig. 4. Two examples of ICS cells. (a). 2-terminal ICS cell in Fig. 2 (j). (b). 3-terminal ICS cell in Fig. 2 (a).

IV TRANSLATION BETWEEN THE 2-TERMINAL AND 3-TERMINAL ICS CELLS

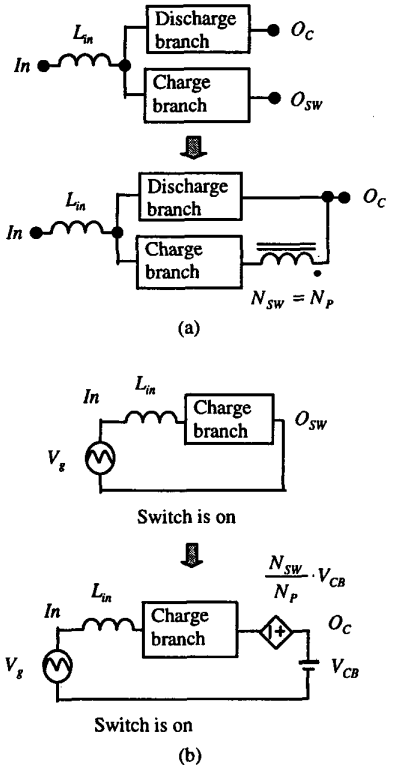


Fig. 5. Translation from 3-terminal ICS cell to 2-terminal ICS cell. (a). Adding one additional winding. (b) Equivalent circuit when switch is on.

A 3-terminal ICS cell can be translated to a 2-terminal ICS cell by adding one extra winding and vise versa, while the electrical property of the converter remains unchanged. The translation principle is shown in Fig. 5. The polarity of the added winding should be such that the equivalent circuit before and after the translation is the same when the switch is on, as shown in Fig. 5 (b). The number of turns of the added winding should equal that of primary winding of the transformer in the dc-dc converter. The discharge branch remains same before or after translation.

From Fig. 5, it is clear that the electrical property of the input current shaper cell does not change by adding one extra winding because the added voltage cancels the voltage across the capacitor voltage. Therefore, the two circuits shown in Fig. 5 are equivalent. Likewise, a 2-terminal ICS cell can be translated to a 3-terminal cell by adding one extra winding in the charge branch and connect the charge branch to switch in dc/dc converter. The principle is shown in Fig. 6. The polarity of the winding is reversed compared to that in Fig. 5.

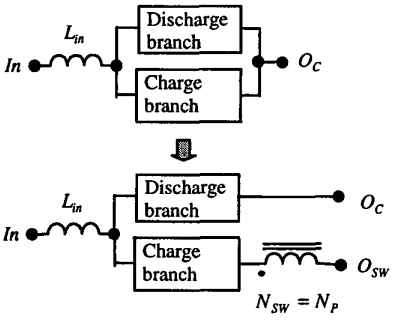


Fig. 6. Principle of translation from 2-terminal ICS cell to 3_terminal ICS cell.

V APPLICATION OF THE TRANSLATION RULES

A Equivalent relationship among existing single-stage PFC topologies

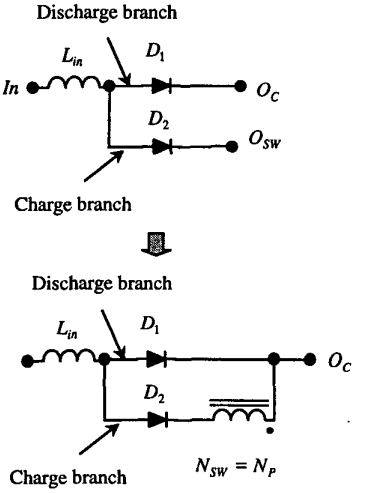


Fig. 7. Translation from the 3-terminal cell in Fig. 2 (a) to the 2-terminal cell in Fig. 2 (j)

According to the observed rules for translation between a 2-terminal and a 3-terminal ICS cell, many of published single-stage PFC converters are electrically equivalent. For example, the 3-terminal ICS cell in the single-stage PFC shown in Fig. 2 (a) can be translated to a 2-terminal cell as shown in Fig. 7. This procedure yields a different single-stage PFC topologies as shown in Fig. 2 (j). Fig. 7

shows that circuits in Fig 1(a) and (j) have equivalent electrical property although published by different authors.

B Derive new rectifiers from existing single-stage PFC rectifiers

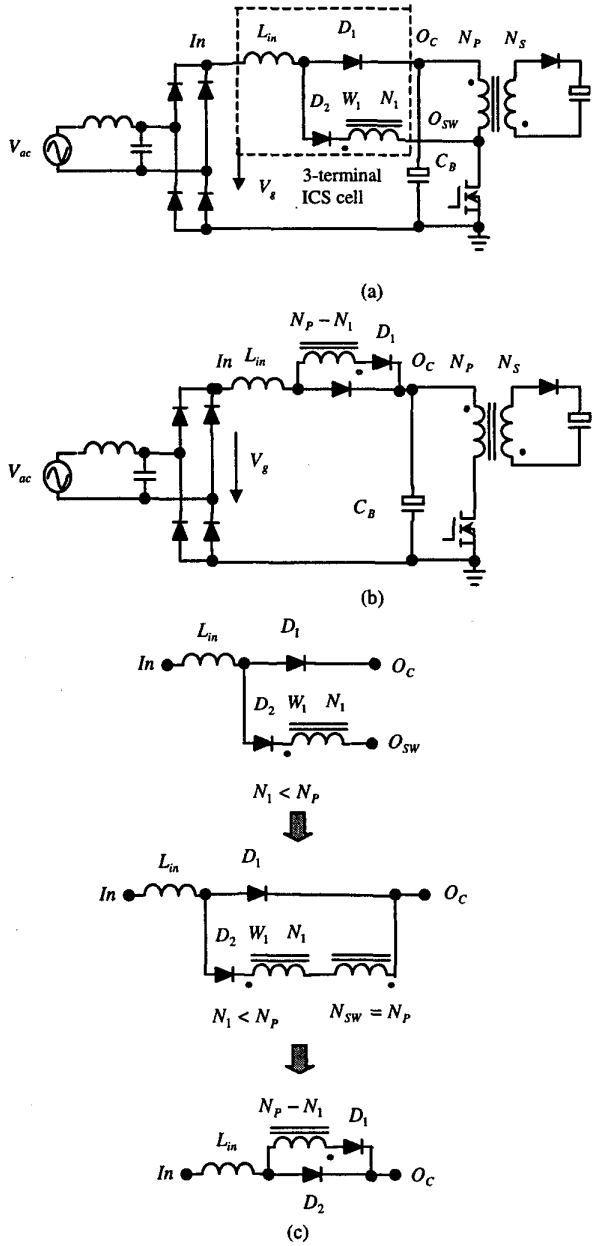


Fig. 8. Derive a new single-stage PFC topology by translating the 3-termnal ICS cell to 2-terminal ICS cell. (a). Proposed single-stage PFC in [17]. (b). The generated equivalent single-stage PFC for the converter in (a) or Fig. 2 (b). (c) The translation from 3-terminal ICS cell in (a) to 2-terminal ICS cell in (b).

For a single-stage PFC with 2 (or 3)-terminal ICS, there exists an equivalent topology with 3 (or 2)-terminal ICS cell according to the observed rules. The single-stage PFC with an extra winding in Fig. 2 (b) [17] is redrawn in Fig. 8 (a). The generated new single-stage converter by translating the 3-terminal ICS cell to a 2-terminal ICS cell is shown in Fig. 8 (b). The translation procedure is shown in Fig. 8 (c). PSPICE simulation and experiments verify that these two topologies have the same input current waveforms under the same working condition.

The generalized 2-terminal and 3-terminal ICS cells are listed in Table 1 of APPENDIX. The two cells in each row are electrically equivalent according to the observed translation rules between 2-terminal and 3-terminal ICS cells. The ICS cells boxed by dashed line are generated with proposed rules.

VI CONCLUSION

A review of single stage PFC rectifiers is given in this paper. From energy flow point of view, the single-stage PFC can be categorized into two major groups: cascade and parallel connected single-stage PFC. Both of them can achieve fast output response and power factor correction. In the parallel-connected single-stage PFC, one portion of the energy is transferred to the load directly, the other portion of energy is processed twice in order to get a fast output load response. These type of PFC rectifiers have higher overall efficiency, but in general they require more semiconductor switches and complicated control circuit.

The cascade-connected single-stage PFC usually integrates a boost or buck-boost input current shaping cell and a forward or flyback converter with an energy storage capacitor in between. The energy is processed twice, but the only one switch is required in most cases. The energy storage capacitor is found in either parallel or series path of energy flow. The cascade-connected single-stage PFC with a capacitor in parallel path of energy flow seems to be dominant. Most of the representatives of these topologies are closely investigated in this paper. These converters can be configured by inserting a 2-terminal or 3-teminal ICS cell between the input diode bridge and dc-dc converter. An energy storage capacitor is inserted in between. The ICS cells draw near sinusoidal current from ac source and improve the power factor. A general rule is observed that allow the translation between 2-terminal and 3-terminal ICS cells. Using these rule, we found that many reported single-stage PFC converters are electrically equivalent despite that they are topologically different, because they employ equivalent ICS cells although their configurations are different. Furthermore, according to the observed rules, several new single-stage topologies were derived by translating existed 2 (or 3)-terminal ICS cell to 3 (or 2)-terminal ICS cell. Although the dc/dc converter analyzed in this paper is flyback converter, the generalized ICS cells are applicable to other topologies as well such as forward converter, etc.

REFERENCES:

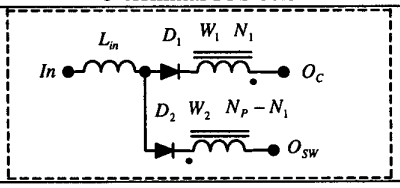
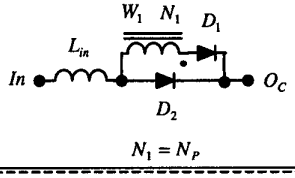
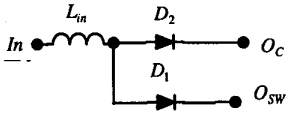
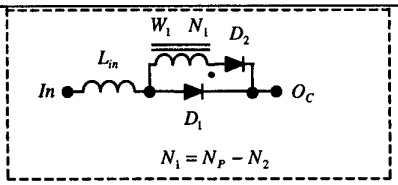
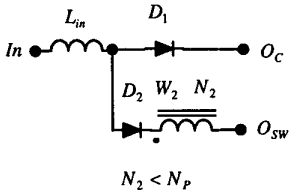
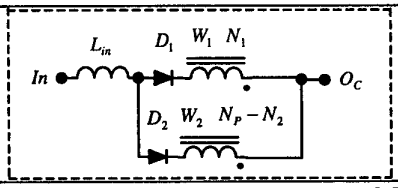
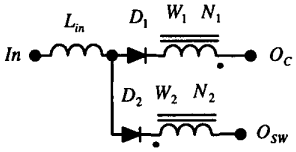
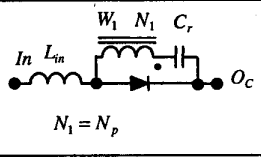
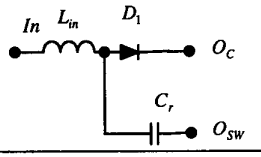
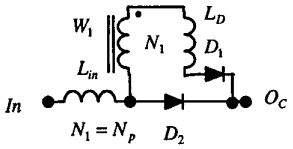
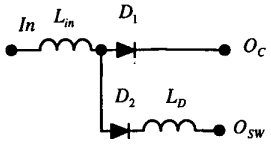
[1] Freeland S. "Input Current Shaping for Single-Phase AC-DC Power Converters" Part II of Ph.D. Thesis Caltech, 1988.

[2] Sharifipour, B.; Huang, J.S.; Liao, P.; Huber, L.; Jovanovic, M.M. "Manufacturing and cost analysis of power-factor-correction circuits". IEEE Applied Power Electronics Conf. (APEC), p.490-4 vol.1, 1998.

[3] Jindong Zhang; Jovanovic, M.M.; Lee, F.C. "Comparison between CCM single-stage and two-stage boost PFC converters". APEC '99, p.335-41.
[4] Kheraluwala, M.H.; Steigerwald, R.L.; Gurumoorthy, R. A fast-response high power factor converter with a single power stage. PESC '91 Record.
[5] Takahashi, I.; Igarashi, R.Y. A switching power supply of 99% power factor by the dither rectifier. Thirteenth International Telecommunications Energy Conference - INTELEC 91.
[6] Madigan, M.; Erickson, R.; Ismail, E. "Integrated high quality rectifier-regulators". PESC '92, p.1043-51.
[7] Brkovic, M.; Cuk, S. Automatic Current Shaper with Fast Output Regulation and SoftSwitching" INTELEC'93. .
[8] Schenk, K.; Cuk, S. A single-switch single-stage active power factor corrector with high quality input and output. PEPSC97 Record.
[9] M. M. Jovanovic, D. M. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency control", IEEE APEC, 1994, pp. 569-575.
[10] Redl, R.; Balogh, L.; Sokal, N.O. "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage". PESC '94. P1137-1144.
[11] Lee, Y.S.; Siu, K.W. Single-switch fast-response switching regulators with unity power factor. APEC '96.
[12] Chow, M.H.L.; Lee, Y.S.; Tse, C.K. "Single-stage single-switch isolated PFC regulator with unity power factor, fast transient response and low voltage stress". PESC 98, p1422-1428.
[13] Chow, M.H.L.; Siu, K.W.; Tse, C.K.; Yim-Shu Lee A novel method for elimination of line-current harmonics in single-stage PFC switching regulators. IEEE Transactions on Power Electronics, vol.13, (no.1), IEEE, Jan. 1998. p.75-83.
[14] R. Redl and L. Balogh, " Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage", ". IEEE Applied Power Electronics Conf. (APEC), p454-458, 1995.
[15] Mei Qiu; Moschopoulos, G.; Pinheiro, H.; Jain, P. "Analysis and design of a single stage power factor corrected full-bridge converter". APEC '99, p.119-25 vol.1.
[16] Rodriguez, E.; Canales, F.; Najera, P.; Arau, J. A novel isolated high quality rectifier with fast dynamic output response. PEPSC97, p.550-5 vol.1.
[17] Fu-Sheng Tsai; Markowski, P.; Whitcomb, E. Off-line flyback converter with input harmonic current correction. INTELEC'96, p.120-4.
[18] Jinrong Qian; Qun Zhao; Lee, F.C. Single-stage single-switch power-factor-correction AC/DC converters with DC-bus voltage feedback for universal line applications. IEEE Transactions on Power Electronics, vol.13, (no.6), IEEE, Nov. 1998. p.1079-88.
[19] Qun Zhao; Lee, F.C.; Fu-Sheng Tsai. "Design optimization of an off-line input harmonic current corrected flyback converter". APEC '99. p p.91-7
[20] Hubber, L; Jovanovic, M.M. "Design optimization of single-stage, single-switch Input-current shapers", IEEE Power Electronics Specialists Conference, 1997, p.519-26 vol.1.
[21] Huber, L.; Jovanovic, M.M. Single-stage, single-switch, isolated power supply technique with input-current shaping and fast output-voltage regulation for universal input-voltage-range applications. APEC '97, p272-80.
[22] Huber, L.; Jovanovic, M.M. "Single-stage single-switch input-current-shapping technique with fast-output-voltage regulation", IEEE trans. On Power Electronics, vol.13, May 1998. P476-486.
[23] Jinrong Qian; Lee, F.C.Y. A high-efficiency single-stage single-switch high-power-factor AC/DC converter with universal input. IEEE Transactions on Power Electronics, vol.13, (no.4), July 1998. p.699-705.
[24] Sebastian, J.; Hernando, M.M.; Villegas, P.; Diaz, J.; Fontan, A. Input current shaper based on the series connection of a voltage source and a loss-free resistor. APEC '98.
[25] Sebastian, J.; Hernando, M.M.; Villegas, P.; Diaz, J.; Fontan. "A new input current shaping technique using converters operating in continuos conduction mode", PESC'98. P1330-6.
[26] Fernandez, A.; Sebastian, J.; Linera, F.F.; Alvarez, L.; Arau, J. Single stage AC-to-DC converter with self-driven synchronous rectification that complies with IEC-1000-3-2 regulations. APEC '99, p 105-11.
[27] Jindong Zhang; Lee, F.C.; Jovanovic, M.M. An improved CCM single-stage PFC converter with a low-frequency auxiliary switch. APEC '99. p.77-83 vol.1.
[28] Sebastian, J.; Fernandez, A.; Villegas, P.; Hernando, M.M.; Ollero, S. Design of an AC-to-DC converter based on a flyback converter with active input current shaper. APEC '99. p.84-90.
[29] Watanabe, H.; Kobayashi, Y.; Sekine, Y.; Morikawa, M.; Ishii, T. The suppressing harmonic currents, MS (magnetic-switch) power supply. International Telecommunications Energy Conference (INTELEC), 1995, p.783-90.
[30] Matsuo, H.; Tu, L.; Kurokawa, F.; Watanabe, H. " A novel soft-switching buck-boost type AC-DC converter with high power efficiency, high power factor and low harmonic distortion". PESC 98. P1030-5.
[31] Daniele, M.; Jain, P.; Joos, G. A single stage power factor corrected AC/DC converter. INTELEC'96. p.256-62
[32] Jain, P.K.; Espinoza, J.R.; Ismail, N.A. " A single-stage zero-voltage zero-current-switched full-bridge DC power supply with extended load power range". IEEE Transactions on Industrial Electronics, vol.46, (no.2), IEEE, April 1999. p.261-70.
[33] Moon, G.-W. Novel single-stage, single-switch, AC/DC converter with magnetic energy feedback technique for power factor correction. IEE Proceedings-Electric Power Applications, vol.146, (no.1), IEE, Jan. 1999. p.111-16. 7.
[34] Jiang,Y and Lee, FC, "Single-stage single-phase parallel power factor correction scheme" PESC'94, p.1145-51 vol.2.
[35] Zheren Lai; Smedley, K.M. A single-stage power-factor-corrected AC-DC converter with fast output regulation and improved current shaping. Official Proceedings of the Twelfth International HFPC Power Conversion, 1997. p.51-62.
[36] Kornetzky, P.; Huai Hei; Batarseh, I. "A novel one-stage power factor correction converter". APEC '97. p.251-8 vol.1.
[37] Kornetzky, P.; Huai Wei; Guangyong Zhu; Batarseh, I. A single-switch AC/DC converter with power factor correction. PEPSC97. p.527-35 vol.1.
[38] Y. k. Cha, M.H. Ryu; B.C. Choi, H.G. Kim. "Single stage AC/DC converter with low conduction loss and high power factor". PESC'98, p1362-7. (acL)
[39] Jun-Young Lee; Gun-Woo Moon; Myung-Joong Youn "Design of high quality AC/DC converter with high efficiency based on half bridge topology". PESC 98, p1054-1060 (synrectifier)
[40] Y.S. Lee; K.W. Siu; B.T. Lin. "Novel single-stage isolated power-factor-corrected power supplies with regenerative clamping", APEC 97, p259-65.
[41] Tse and Chow, "Single stage high power factor converter using the Sheppard-Taylor topology." PESC96.
[42] Garcia, O.; Cobos, J.A.; Alou, P.; Prieto, R.; Uceda, J.; Ollero, S. A new family of single stage AC/DC power factor correction converters with fast output voltage regulation. PEPSC97, p.536-42 vol.1.
[43] Garcia, O.; Cobos, J.A.; Alou, P.; Prieto, R.; Uceda, J.; Ollero, S. " A high efficient low output voltage(3.3v) single-stage AC/DC power factor correction converter", APEC'98, p.201-7.
[44] Garcia, O.; Cobos, J.A.; Alou, P.; Prieto, R.; Uceda, J.; Ollero, S. " A new approach for single stage AC/DC power factor correction converters with an improved energy processing", PESC'98, p1061-7.
[45] Rodriguez, E.; Garcia, O.; Cobos, J.A.; Arau, J.; Uceda, J. A single-stage rectifier with PFC and fast regulation of the output voltage. PESC 98, p1642-8.
[46] T.F. Wu; T.-H. Yu and Y.C. Liu. " Principle of synthesizing single-stage converters for off-line applications". APEC'98, p427-433.
[47] T.F. Wu; Y-J Wu, and Y.C. Liu, Development of Converters for Improving Efficiency and Achieving Both Power FactorCorrection and Fast Output Regulation. APEC'99.
[48] Jindong Zhang; Huber, L.; Jovanovic, M.M.; Lee, F.C. Single-stage input-current-shaping technique with voltage-doubler-rectifier front end. APEC '99, p112-9.

APPENDIX

Table 1. The generalized 2-terminal and 3-terminal ICS cells.

	2-terminal ICS cell	3-terminal ICS cell
DCM ICS cells		
(a)		
(b)		
(c)		
(d)		
CCM ICS cells		
(e)		
(f)		
(g)